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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/535,448	09/19/2005	Wolfgang Clemens	411000-131	6015

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EXAMINER

SARKAR, ASOK K

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2891

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/535,448	Applicant(s) CLEMENS ET AL.	
	Examiner Asok K. Sarkar	Art Unit 2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4 and 6-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4 and 6-19 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>9/05;10/05;5/07</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 4 and 6 – 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Arai, US 2004/0075093.

Regarding claim 1, Arai teaches an organic electronic component with a patterned upper functional layer 106 having a thickness of at most about 100 nm (paragraphs 41 and 47) deposited on one of a lower layer 102 and a substrate layer 101, the component being formed by patterning the upper functional layer 106 by treatment of the one layer in which a first partial region of the one layer is wetted by the upper functional layer when applied to the one layer and a second partial region of the one layer is not wetted by the deposited upper layer and therefore is free of the functional layer to thereby pattern the upper functional layer 106 (Fig. 1) on the lower layer with reference to Figs. 1 and 2 especially Fig. 2E in paragraphs 38 – 52. This is a product by process claim.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this

issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 2, Arai teaches the patterned functional layer 106 is a semiconducting functional layer in paragraph 45.

Regarding claim 6, Arai teaches an organic electronic component comprising:

- a substrate 101;
- one of a lower functional layer 102 and a lower substrate layer 101 having a predetermined area; and
- a patterned functional upper layer 106 on the one lower layer having a thickness at most of about 100 nm, the one lower layer including an arrangement 105 to prevent wetting by the upper layer in the predetermined area as the patterned functional upper layer is applied to the one lower layer including the predetermined area so that the upper layer only partially wets the lower layer to form a lower layer region free of the upper layer in the predetermined area with reference to Fig. 1 as was discussed earlier in rejecting claim 1. The surface properties of the resist mask and the insulating gate electric surface (Figs. 2B and 2C) will be inherently different to provide different wetting characteristics for the liquid semiconductor film. This is a product by process claim.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this

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issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 7, Arai teaches an organic electronic component comprising:

- one of a lower functional layer and a lower substrate layer having a given area;
and

- a patterned functional upper layer on the one lower layer having a thickness at most of about 100 nm, the one lower layer being formed by an arrangement to prevent wetting by the upper layer of at least a portion of the given area so that the upper layer only partially wets the lower layer to form the pattern with

reference to Fig. 1 as was described earlier in rejecting claims 1 and 6. This is a product by process claim.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claims 8 and 9, Arai teaches the one lower layer includes an arrangement to prevent the wetting by the upper layer due to the different surface properties of the two materials as were explained earlier in rejecting claim 6.

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Regarding claim 10, Arai teaches an organic electronic component comprising:
forming one of a lower functional layer and a lower substrate layer ; applying an upper functional layer to the one lower layer; and preventing the applied upper functional layer from wetting the one lower layer in at least a portion of the one lower layer to form the applied upper layer into a pattern on the one lower layer with reference to Fig. 1 as was explained earlier in rejecting claims 1, 6 and 7. This is a product by process claim.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 4, Arai teaches the applied upper layer comprises a patterned semiconducting functional layer 106 with reference to Fig. 1.

Regarding claims 11 and 12, Arai teaches forming/printing a resist layer (printing a treatment) on the portion of the lower layer with reference to Fig. 2B. These are products by process claims and therefore the processing limitations are not given any patentable weight.

Regarding claim 13, Arai teaches a circuit formed of organic functional layers comprising:

a substrate 301;

and a plurality of adjacent organic electronic components on the substrate, each component comprising one or more conductive functional layer electrodes 302 and a patterned semiconducting layer 305 on the one or more electrodes;

the patterned semiconducting functional layer having a thickness no greater than about 100 nm, the patterned semiconducting functional layer having an electrical interruption between next adjacent components with reference to Figs. 1 and 4A – 4D in paragraphs 38 – 52 and in paragraphs 53 – 59.

Regarding claim 14, Arai teaches the electrical interruption comprises a semiconducting free area 304 on the substrate with reference to Fig. 4A.

Regarding claim 15, Arai teaches at least one of the components is a transistor with reference to Figs. 1 and 4A.

Regarding claims 16 – 19, Arai teaches the limitations of these claims as have been described earlier in rejecting claims 7 – 12.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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4. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Asok K. Sarkar/
Primary Examiner, Art Unit 2891

January 31, 2008